SANT GADGE BABA AMARAVATI UNIVERSITY, AMARAVATI.
SUMMER EXAMINATION-2020
H.V.P.M.'s College of Engineering and Technology, Amravati.
Department of Electronics and Telecommunication
Bachelor of Engineering Semester IV.

Subject : Digital Electronics – I **Subject code : 4ET4**

Instructions:-

i) Solve any two questions.

ii) ii) All questions carry equal marks.

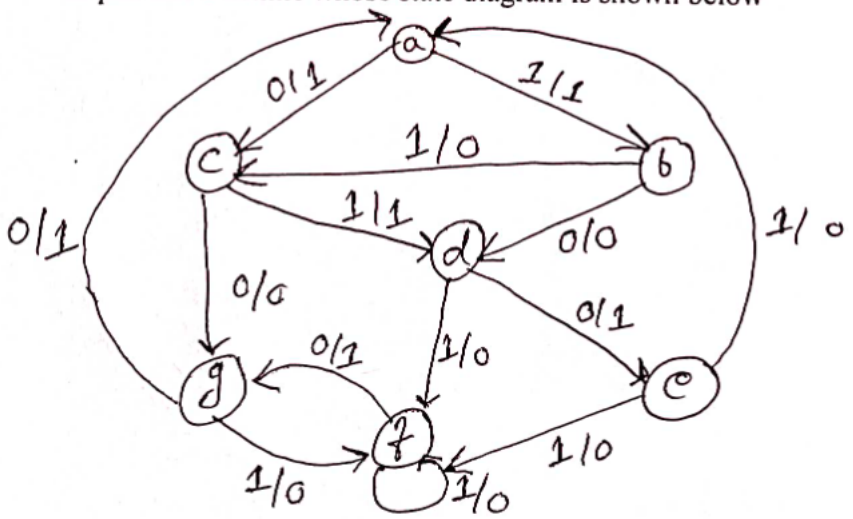
Que 1 **a)** Explain **in brief** Transistor-Transistor logic {TTL) **circuit** with active **pull up** arrangements. Verify the logic operations given by TTL — 2 credit pts

b) Minimize the following logic function and realize using NAND gates only. f| (A, B, C, D)= $\sum$ m (l,3,5,8,9,11,15) +d(2,13) — 2 credit pts

c) Implement the following logical expression using 8:1 MUX
F = $\sum$ m (0,1, 2,3,4,10,l l,l4,l5) — 2 credit pts

d) What is Race around condition? I low it is overcome? Explain master-slave I-K flip flop with proper table — 2 credit pts

e) Obtain reduced stale table and reduced state diagram for the sequential machine whose state diagram is shown below — 1 credit pts



f) Explain in brief (i) PROM (ii) EEPROM (iii) EPROM — 1 credit pts

Que 2 a) Perform the following using 2's compliment method — 2 credit pts

(1) $(48)_{10} - (23)_{10}$

(2) $(48)_{10} - (-23)_{10}$

(3) $(-48)_{10} - (23)_{10}$

b) Design the combinational circuit for full adder God implements it using suitable gates. — 2 credit pts

c) Design 5-line to 32 line decoder circuit using 4-line to 16-line decoders and suitable gate. — 2 credit pts

d) Design 4-bit parallel in serial out right shift register using D-Flip Flops and suitable gates. — 2 credit pts

e) The state diagram and state table for a Moore type sequence detector to detect the sequence 11 10 — 1 credit pts

f) Explain the working of dynamic RAM cell. — 1 credit pts

Que 3 a) 1)Perform the following: — 2 credit pts

(i) $(BC5)_{16} - (A2B)_{16} = (?)_2$, (ii) $(287)_{10} = (?)_{gray}$

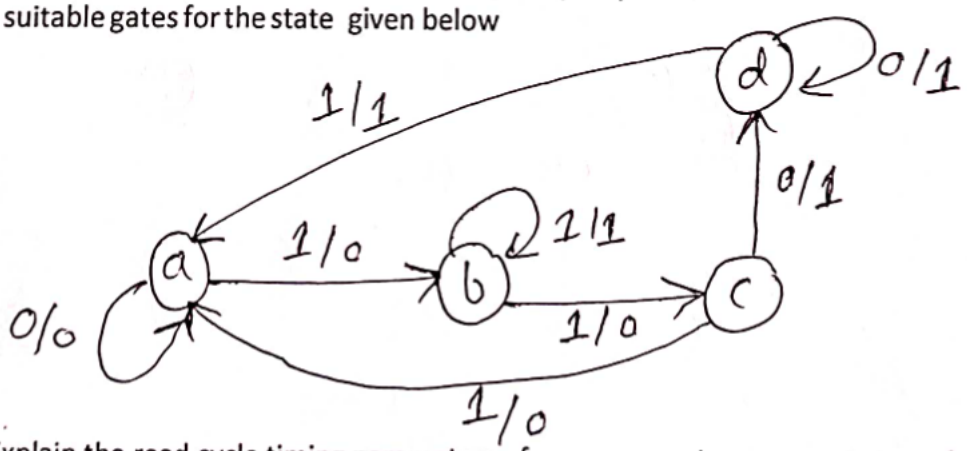
(iii) $(0.65625)_{10} = (?)_2$ (iv) $(327.89)_{10} = (?)_{BCD}$

b) Design and explain one digit BCD adder circuit using 4-bit adder IC 74LS83 and required gates. Explain with the help of suitable example. — 2 credit pts

c) Design 5-bit comparator using single 7485 IC and suitable gate. Also explain its operation — 2 credit pts

d) State differences between synchronous and asynchronous counters, — 2 credit pts

e) Design a clocked sequential circuit using T-Flip Flops and suitable gates for the state given below — 1 credit pts



f) Explain the read cycle timing parameters of a memory using proper timing diagram — 1 credit pts

Que 4

a) Explain TTL with active pull up. Give its significance. 2 credit pts

b) Design binary to gray code converter circuit using suitable gate . 2 credit pts

c) The truth table for an ROM to implement the given function :
$f=\sum m(1,2,4,6)$ 2 credit pts

d) Design a synchronous counter to count the sequence 1-2-5-3-0-7 using T- F-F. 2 credit pts

e) Define an asynchronous sequential circuits . How its differs from synchronous sequential circuits. 1 credit pts

f) With neat circuit diagram explain the operation of bipolar static RAM Cell 1 credit pts