SANT GADGE BABA AMRVATI UNIVERSITY, AMRAVATI
Summer Examination 2020 Credit Point
HVPM's College of Engineering and Technology, Amravati
Department of Electronics & Tele communication Engineering
Bachelor of Engineering Sem. :- VI

Subject :-Digital Integrated Circuits **Code :- 6XT1**

Instructions:-

1) **Solve any two questions**
2) **All question carry equal marks**

Q1.

a) Design a 3 input combinational ckt. Where o/p is equal to 1 if the i/p Variable have more 1's than 0's , otherwise logic 0 **02 Credit Point**

b) Design 32:1 mux using 4:1 Mux **02 Credit Point**

c) Design the look ahead carry adder and explain its operation **02 Credit Point**

d) Convert S-R FF to J-K FF **02 Credit Point**

e) What are races . Explain critical and non critical races . **01 Credit Point**

f) State and explain the condition under which faults can't be located **01 Credit Point**

Q2.

a) Prove that SOP and POS expression are equivalent for bit systems with suitable example **02 Credit Point**

b) Design 10 bit odd parity generator using IC 74180 **02 Credit Point**

c) Explain the working of FPGA **02 Credit Point**

d) Explain how SM chart differs from a conventional flowchart using suitable example. **02 Credit Point**

e) Explain various hazards in asynchronous circuits . Explain how static 0 hazards can be eliminated **01 Credit Point**

f) Explain how two level faults can be detected . Illustrate with suitable examples. **01 Credit Point**

Q3.

a) Simplify the following expression and realize using NOR / NAND gate only. **02 Credit Point**

1) F1= $\sum m(1,3,5,8,9,11,15) + d(2,13)$

2) F2= $\prod M(1,2,3,8,9,10,11,14) \cdot d(7,15)$

b) Design 8 bit comparator using IC 7485 with truth table **02 Credit Point**

c) The truth table for an ROM to implement the given function : $f=\sum m(1,2,4,6)$ **02 Credit Point**

d) Design a synchronous counter to count the sequence 1-2-5-3-0-7 using T- F-F. **02 Credit Point**

e) Define an asynchronous sequential circuits . How its differs from synchronous sequential circuits. **01Credit Point**

f) Explain fault detection by ckt. Test approach **01Credit Point**

Q4.

a) Simplify the following logic function using Quine-Mc Cluskey minimization technique. $F(A,B,C,D) = \sum m(1,4,9,10,15) + d(6,7,8,11)$ **02 Credit Point**

b) Design EX-3 to BCD code converter **02 Credit Point**

c) Explain ROM as ROM **02 Credit Point**

d) Differentiate between Mealy model and Moore of a sequential circuit **02 Credit Point**

e) Explain the following with respects to an asynchronous sequential ckt. (i) primitive flow table (ii) Merger diagram **01 Credit Point**

f) Find minimal test set to detect all faults in the ckt. Shown **01 Credit Point**