SANT GADGE BABA AMRVATI UNIVERSITY, AMRAVATI
Summer Examination 2020
HVPM's College of Engineering and Technology, Amravati
Department of Electronics & Tele communication Engineering
Bachelor of Engineering Sem. :- VII

Subject :- VLSI DESIGN **Code :-** 7XT04(10630)

Instructions:-

1) **Solve any two questions**
2) **All question carry equal marks**

Q1.

a) Explain advantages and applications of VLSI. **02 Credit Point**

b) Using suitable examples explain various modeling styles used in VHDL which style is said to be 'target technqlogy independent' and why? **02 Credit Point**

a) Develop a VHDL code for 2:4 decoder in structural type of modeling **02 Credit Point**

b) Cornpare CPLD and FPGA **02 Credit Point**

c) With the help of neat sketch. Explain physical structure of MOS transistor **01 Credit Point**

d) Explain n. well process with suitable diagrams **01 Credit Point**

Q2.

a) What is difference between combinational and sequential circuit**.** **02 Credit Point**

b) Explain the following with example :
(i) process
(ii) case
(iii) if
(iv) loop. **02 Credit Point**

c) Explain predefined Attributes used in VHDL.
02 Credit Point

d) Draw and explain architecture of CPLD **02 Credit Point**

e) What are the advantages of CMOS logic families over the other logic families ?
01 Credit Point

f) Explain MESi protocol **01 Credit Point**

Q3.

a) What is Moore's law? Explain it in brief. **02 Credit Point**

b) Expalin VLSI Design flow in detail **02 Credit Point**

c) Compare function and procedure used in VHDL **02 Credit Point**

d) Explain switch matrix in CPLD **02 Credit Point**

e) Explain DC characteristics of CMOS inverter. **01 Credit Point**

f) Explain twin tube process **01 Credit Point**

Q4.

a) Explain IP Life cycle in detail. **02 Credit Point**

b) Write a VHDL code for 3 : 8 decoder using data flow style of modeling. **02 Credit Point**

c) How generics arc used in VHDL ? Explain in detail with suitable example. **02 Credit Point**

d) Explain Altera max 7000 CPLD **02 Credit Point**

e) Draw and explain the basic CMOS layout for NOR gate **01 Credit Point**

f) Explain λ based design rule for manufacturing of CMOS circuits. **01 Credit Point**