SANT GADGE BABA AMRAVATI UNIVERSITY,AMRAVATI
HanumanVyayamPrasarak Mandals's
College of Engineering & Technology, Amravati
Course:Information Technology
BE Four year Semester(Information technology) Summer 2020 Exam
Subject: 5IT02 Digital Integrated Circuits
Assignment for ONLY BACKLOG STUDENTS

Instructions

1) **Solve ANY TWO Questions**
2) **Each Question Carries 10 marks**

QI)Solve the following

1) Draw the Tree Diagram of Logic families [2M]

2) Explain basic logic gates [2M]

3)Draw truth table for Half Adder [1M]

4)Implement the function $f(x,y,z)=\sum m(1,2,4,5)$ using 4:1 MUX [2M]

5) Draw truth table for D flip flop [1M]

6)Draw Bipolar RAM Cell [2M]

Q II) Solve the following

1)Draw the symbol of N-channel &P-channel Depletion & Enhancement type MOSFET [2M]

2) Explain Derived logic gates [2M]

3) Draw truth table for Half substractor [1M]

4)Draw truth table for magnitude comparator with 3 output A>B, A=B, A<B using logic gates. [2M]

5) Draw the truth table for T-flip flop [1M]

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6) Draw MOS Static RAM Cell [2M]

QIII) Solve the following

1) Draw the circuit diagram of TTL as NAND Gate [2M]
2) Draw only K-Map for SOP form f = πM(0,3,6,9,12,15) [2M]
3) Draw truth table for full Adder [1M]
4) Draw 4 bit binary adder substractor circuit [2M]
5) Draw the truth table for S-Rflip flop [1M]
6) Compare SRAM and DRAM [2M]

QIV) Solve the following

1) Define power dissipation and propogation delay [2M]
2) Minimize the 4 variable logic function using K-map f= πM (0,2,3,6,7,8,9,12,13) [2M]
3) Draw the truth table for full substractor [1M]
4) Design 5:32 line Decoder using 4:16 line decoder. [2M]
5) Draw the truth table for J-K flip flop [1M]
6) What are the 4 types of modes of operation of shift register [2M]